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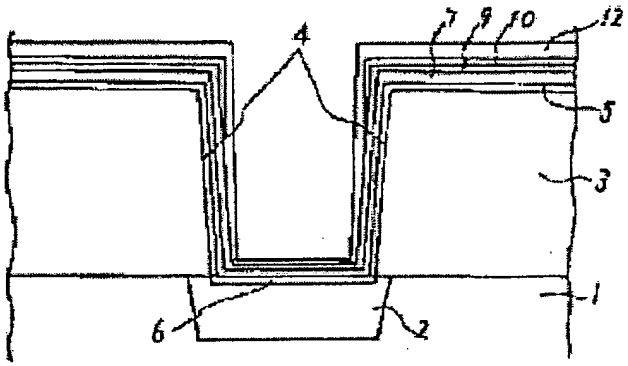
Abstract of **JP9213656**

PROBLEM TO BE SOLVED: To enable a control of the eutectic reaction of an Al film to a titanium film and to bury a conductive layer in a high-aspect ratio open part with good accuracy by a method wherein a reaction preventive film is formed on the upper surface of the titanium film extending from the prescribed height of the sidewall of the open part to the upper surface of an interlayer insulating film.

SOLUTION: A TiN film 10, which is a reaction preventive film, is selectively formed on the upper surface of an interlayer insulating film 3 and the upper part of the sidewall in the interior of a contact hole 4. Thereby, a Ti film 9 only being exposed in the interior of the hole 4 reacts with an Al film 12. Accordingly, the excessive eutectic reaction of the film 12 to the film 9 can be prevented from being generated. Moreover, as the existing part of the film 9, which reacts, is limited, the Ti film 9, which acts, can be controlled by controlling the film thickness of the film 9 situated at the part. Accordingly, a control of the eutectic reaction becomes possible and the hole can be filled with the film 12 with good accuracy.



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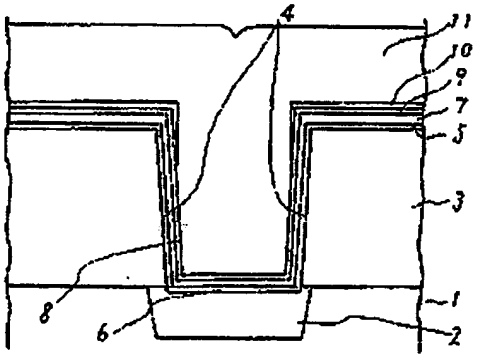
(54)【発明の名称】　半導体装置およびその製造方法

(57)【要約】

【課題】　高アスペクト比開口部にＡｌ膜１１を埋め込む工程において、Ａｌ膜１２とＴｉ膜９との共晶反応を利用しているが、共晶反応の制御が難しく埋め込みが不十分になる。

【解決手段】　Ｔｉ膜９とＡｌ膜１２との間の一部分に、反応防止膜であるＴｉＮ膜１０を形成した。

【効果】　Ｔｉ膜９の一部分をＴｉＮ膜１０で覆って共晶反応させたので、共晶反応の制御が可能になり、開口部へのＡｌ膜１１の埋め込み精度が向上する。



1：基板　7：TiN膜
3：層間絶縁膜　8：共晶膜
4：コンタクトホール　9：第1のTi膜
5：第2のTi膜　10：TiN膜
6：チタンシリサイド層　11：第1のAl膜

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【特許請求の範囲】

【請求項１】　下部導電層の上層に層間絶縁膜が形成され、前記層間絶縁膜に開口部が形成され、前記開口部に導電体を埋め込んで前記下部導電層と電気的に接続された上部導電層を備えた半導体装置において、前記上部導電層が、前記開口部の底部から側壁の所定の高さにまで形成されたチタンとアルミニウムまたはその合金との共晶膜と、前記開口部の側壁の所定の高さから前記層間絶縁膜の上面にかけて下層から順に形成された第１のチタン膜と前記第１のチタン膜とアルミニウムまたはその合金との共晶反応を防止する反応防止膜との積層膜と、前記積層膜と前記共晶膜との上層に形成された第１のアルミニウムまたはその合金膜とで構成されていることを特徴とする半導体装置。

【請求項２】　反応防止膜が、チタンの窒化膜、酸化膜または窒酸化膜であることを特徴とする請求項１記載の半導体装置。

【請求項３】　層間絶縁膜の上層には第２のチタン膜が、開口部の底部に露出している下部導電層の表層部にはチタンシリサイド層がそれぞれ形成され、前記第２のチタン膜と前記チタンシリサイド層との上層にはチタン窒化膜が形成され、前記チタン窒化膜の上層に積層膜および共晶膜が形成されていることを特徴とする請求項１または２記載の半導体装置。

【請求項４】　下部導電層の上層に層間絶縁膜を形成する工程と、前記層間絶縁膜の所定の位置に開口部を形成する工程と、前記開口部の内部を含む全面に第１のチタン膜を形成する工程と、前記開口部の側壁の所定の高さから前記層間絶縁膜の上面にかけての前記第１のチタン膜の上層に反応防止膜を形成する工程と、前記第１のチタン膜と前記反応防止膜との上層に第２のアルミニウムまたはその合金膜を形成する工程と、前記第２のアルミニウムまたはその合金膜の上層に第１のアルミニウムまたはその合金膜を形成すると同時に、前記開口部の底部から側壁の所定の高さにまでチタンとアルミニウムまたはその合金膜との共晶膜を形成する工程とを備えた半導体装置の製造方法。

【請求項５】　反応防止膜が、チタンの窒化膜、酸化膜または窒酸化膜であることを特徴とする請求項４記載の半導体装置の製造方法。

【請求項６】　第１のチタン膜、反応防止膜、第１のアルミニウムまたはその合金膜および第２のアルミニウムまたはその合金膜の形成方法が、スパッタ法であることを特徴とする請求項４または５記載の半導体装置の製造方法。

【請求項７】　第１のチタン膜から第１のアルミニウムまたはその合金膜を形成するまでの全工程を、大気暴露することなく連続的に行うことを特徴とする請求項４ないし６のいずれかに記載の半導体装置の製造方法。

【発明の詳細な説明】

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【０００１】

【発明の属する技術分野】本発明は半導体装置及びその製造方法に関し、特に層間絶縁膜に形成された開口部の側壁に形成された導電層の構造とその製造方法に関するものである。

【０００２】

【従来の技術】半導体装置（特にＬＳＩ）の高集積化に伴い、その内部配線が微細化して、各内部配線間の電気的な接続に用いられる開口部（例えば、半導体基板とその上部に形成された導電層との接続孔であるコンタクトホール）のアスペクト比は増大する一方である。

【０００３】このような高アスペクト比開口部（以下、コンタクトホールと記す。）に対し、従来のスパッタ法により導電層であるアルミニウムまたはその合金膜（以下、Ａｌ膜と記す。）を形成すると、図９に示すようにコンタクトホール４の内部でＡｌ膜１３に段切れ１４が生じ、回路が正常に動作しないという問題があった。

【０００４】このような問題を解決するために、高温アルミスパッタ技術が開発された。図１２は、従来の高温アルミスパッタ技術によりＡｌ膜１１が形成された半導体装置の断面図である。図において、１は半導体基板（以下、基板と記す。）、２は不純物拡散層、３は層間絶縁膜、４はコンタクトホール、５はチタン膜（以下、Ｔｉ膜と記す。）、６はチタンシリサイド層、７は窒化チタン膜（以下、ＴｉＮ膜と記す。）、８はチタンとアルミまたはその合金との共晶膜（以下、共晶膜と記す。）、１１はＡｌ膜である。

【０００５】また、従来の半導体装置の製造方法は、基板１の主表面に不純物拡散層２と層間絶縁膜３とコンタクトホール４とを形成した後、コンタクトホール４の内部を含む全面にスパッタ法によりＴｉ膜５とＴｉＮ膜７とを形成する。次に熱処理を行い、コンタクトホール４の底部に形成されたＴｉ膜５と基板１とを反応させ、チタンシリサイド層６を形成した後、ＴｉＮ膜７の上層にスパッタ法によりＴｉ膜９とＡｌ膜１２とを形成する（図１０参照）。

【０００６】次に基板１を高温に加熱しながら全面にスパッタ法によりＡｌ膜１１を形成する。この時、Ａｌ膜１１、１２は融点近くに加熱されているため液状化し始める。また、同時にＴｉ膜９とＡｌ膜１２とが共晶反応を起こし、Ａｌ膜１１がこの反応に加担し始めると濡れ性が向上して移動しやすくなりコンタクトホール４に進む（図１１参照）。そして最終的にはコンタクトホール４を埋め込み、表面はＡｌ膜１１の表面張力により平坦化されて、図１２に示す形状となる。

【０００７】

【発明が解決しようとする課題】しかしながら、従来の高温アルミスパッタ技術では、Ａｌ膜１２とＴｉ膜９との共晶反応が少ないと、Ａｌ膜１１がコンタクトホール４へ進むまでに共晶反応が停止し、図１３に示すように

コンタクトホール4の埋め込みが不完全となる。また、共晶反応が過剰に進むと、Al膜11の大部分が共晶膜8となり移動するAl膜11が少なくなり、かつ部分的に共晶膜8が過剰になるとこれが壁となりAl膜11がコンタクトホール4に移動するのを妨げる。従って、図14に示すようにコンタクトホールの埋め込みが不完全となる。このように、共晶反応の制御が難しく精度良く埋め込みを行うことが困難であった。

【0008】この発明は、上記のような問題点を解決するためになされたもので、高アスペクト比開口部に導電層を精度良く埋め込むことができる半導体装置の構造とその製造方法を提供することを目的とする。

【0009】

【課題を解決するための手段】この発明の請求項1に係わる半導体装置は、下部導電層の上層に層間絶縁膜が形成され、前記層間絶縁膜に開口部が形成され、前記開口部に導電体を埋め込んで前記下部導電層と電気的に接続された上部導電層を備えた半導体装置であって、前記上部導電層が、前記開口部の底部から側壁の所定の高さにまで形成されたチタンとアルミニウムまたはその合金との共晶膜と、前記開口部の側壁の所定の高さから前記層間絶縁膜の上面にかけて下層から順に形成された第1のチタン膜と前記第1のチタン膜とアルミニウムまたはその合金との共晶反応を防止する反応防止膜との積層膜と、前記積層膜と前記共晶膜との上層に形成された第1のアルミニウムまたはその合金膜とで構成されている。

【0010】この発明の請求項2に係わる半導体装置は、請求項1において、反応防止膜が、チタンの窒化膜、酸化膜または窒酸化膜である。

【0011】この発明の請求項3に係わる半導体装置は、請求項1または2において、層間絶縁膜の上層には第2のチタン膜が、開口部の底部に露出している下部導電層の表層部にはチタンシリサイド層がそれぞれ形成され、前記第2のチタン膜と前記チタンシリサイド層との上層にはチタン窒化膜が形成され、前記チタン窒化膜の上層に積層膜および共晶膜が形成されている。

【0012】この発明の請求項4に係わる半導体装置の製造方法は、下部導電層の上層に層間絶縁膜を形成する工程と、前記層間絶縁膜の所定の位置に開口部を形成する工程と、前記開口部の内部を含む全面に第1のチタン膜を形成する工程と、前記開口部の側壁の所定の高さから前記層間絶縁膜の上面にかけての前記第1のチタン膜の上層に反応防止膜を形成する工程と、前記第1のチタン膜と前記反応防止膜との上層に第2のアルミニウムまたはその合金膜を形成する工程と、前記第2のアルミニウムまたはその合金膜の上層に第1のアルミニウムまたはその合金膜を形成すると同時に、前記開口部の底部から側壁の所定の高さにまでチタンとアルミニウムまたはその合金膜との共晶膜を形成する工程とを備えている。

【0013】この発明の請求項5に係わる半導体装置の

製造方法は、請求項4において、反応防止膜が、チタンの窒化膜、酸化膜または窒酸化膜である。

【0014】この発明の請求項6に係わる半導体装置の製造方法は、請求項4または5において、第1のチタン膜、反応防止膜、第1のアルミニウムまたはその合金膜および第2のアルミニウムまたはその合金膜の形成方法が、スパッタ法である。

【0015】この発明の請求項7に係わる半導体装置の製造方法は、請求項4ないし6のいずれかにおいて、第1のチタン膜から第1のアルミニウムまたはその合金膜を形成するまでの全工程を、大気暴露することなく連続的に行う。

【0016】

【発明の実施の形態】

実施の形態1．以下、本発明の実施の形態1について、図面を参照して説明する。図1は、実施の形態1に係わる半導体装置の断面図である。図において、1は下部導電層である基板、2は不純物拡散層、3は層間絶縁膜、4は不純物拡散層2の上方の層間絶縁膜3に開口されたコンタクトホール、5は第2のTi膜であるTi膜、6はコンタクトホールの底部に形成されたTi膜（図示せず。）と基板1とが反応して形成したチタンシリサイド層、7はTiN膜、8は共晶膜、9は第1のTi膜であるTi膜、10は反応防止膜であるTiN膜、11は第1のAl膜であるAl膜である。なおチタンシリサイド層6はオーミックコンタクトを形成して基板1とAl膜11とのコンタクト性を良好にし、TiN膜7はコンタクトホールの底部においてAl膜11と基板1との相互作用による接合破壊を防止するためのバリア層であり、共晶膜8は形成時にAl膜11の濡れ性を向上させてコンタクトホール4への埋め込みを良くする。また、TiN膜10は共晶反応を防止する膜であれば酸化チタン膜や窒酸化チタン膜のいずれであってもよい。

【0017】図2～8および図1は、実施の形態1に係わる半導体装置の製造方法を工程を追って順次示した半導体装置の断面図である。

【0018】図2に示すように、不純物拡散層2が形成されている基板1の主表面上に層間絶縁膜3を形成し、次に不純物拡散層2の上方の層間絶縁膜3にコンタクトホール4を形成する。

【0019】次に図3に示すように、コンタクトホール4の内部を含む全面にスパッタ法によりTi膜5（膜厚数10nm）とTiN膜7（膜厚数10～数100nm）とを形成する。

【0020】次に図4に示すように、熱処理（700～800℃）を行い、コンタクトホール4の底部に形成されたTi膜5と基板1とを反応させ、チタンシリサイド層6を形成する。

【0021】次に図5に示すように、TiN膜7の上層にスパッタ法によりTi膜9（膜厚数10nm）を形成

する。

【００２２】次に図６に示すように、Ｔｉ膜９の上層に通常スパッタ法によりＴｉＮ膜１０を形成する。この時通常スパッタ法は段差被覆性が不十分であるので、膜厚を小さくすること（例えば５ｎｍ以下）によりコンタクトホール４の内部では側壁の所定の高さ以上の上部のみに成膜される。

【００２３】次に図７に示すように、全面にスパッタ法により第２のＡｌ膜であるＡｌ膜１２（膜厚数１００ｎｍ）を形成する。

【００２４】次に図８に示すように、基板１を高温（約５００℃）に加熱しながら全面にスパッタ法によりＡｌ膜１１（膜厚数１００ｎｍ）を形成する。この時、Ａｌ膜１１は、Ａｌ膜１２とＴｉ膜９との共晶反応による濡れ性の向上と加熱による液状化とによりコンタクトホール４に追み、最終的にはコンタクトホール４を埋め込み、表面はＡｌ膜１１の表面張力により平坦化されて、図１に示す形状となる。なお、ＴｉＮ膜１０が形成されているので、共晶反応は、コンタクトホール４側壁一定高さ以下の、Ｔｉ膜９が露出している部分のみで生じる（共晶膜８）。

【００２５】本実施の形態１における成膜条件を以下に示す。

Ｔｉ膜形成条件

ＤＣパワー	数ｋＷ
プロセスガス	Ａｒ　数１０ＳＣＣＭ
圧力	数10^{-1}Ｐａ

ＴｉＮ膜形成条件

ＤＣパワー	数ｋＷ
プロセスガス	Ar/N_2　数１０／数１０ＳＣＣＭ
圧力	数10^{-1}Ｐａ

Ａｌ膜形成条件

ＤＣパワー	数ｋＷ
プロセスガス	Ａｒ　数１０ＳＣＣＭ
圧力	数10^{-1}Ｐａ

【００２６】以上のように、反応防止膜であるＴｉＮ膜１０を層間絶縁膜３の上面とコンタクトホール４内部の側壁の上部とに選択的に形成したので、コンタクトホール４内部の露出しているＴｉ膜９のみがＡｌ膜１２と反応する。従って、過剰な共晶反応を防止できる。また反応するＴｉ膜９の存在部分が限定されているので、その部分のＴｉ膜９の膜厚を制御する事により反応するＴｉ量を制御できる。従って、共晶反応の制御が可能になりコンタクトホールをＡｌ膜１１で精度よく埋め込むことができる。

【００２７】なお、Ｔｉ膜５，９とＴｉＮ膜７との形成において通常スパッタ法では段差被覆性が不十分であるので、段差被覆性を改善するためにコリメーションスパッタ法を用いた。また、実施の形態１では本発明をコンタクトホールに用いたが、高アスペクト比開口部であれば、下層と上層との導電層間の接続孔であるヴィアホールについても同様に適応できる。

【００２８】

【発明の効果】この発明の請求項１に係わる半導体装置においては、開口部の側壁の所定の高さから層間絶縁膜の上面にかけての第１のチタン膜の上層に反応防止膜を形成しているので、チタンとアルミニウムまたはその合金との共晶反応の制御が可能になり、開口部への上部導電層の埋め込み精度が向上する。

【００２９】この発明の請求項２に係わる半導体装置においては、反応防止膜をチタンの窒化膜、酸化膜または窒酸化膜としたので、共晶反応を完全に防止できる。

【００３０】この発明の請求項３に係わる半導体装置においては、下部導電層とチタンとアルミニウムまたはその合金との共晶膜との間にチタンの窒化膜が形成されているので、下部導電層とアルミニウムとの相互反応を抑制して接合破壊を防止できる。

【００３１】この発明の請求項４に係わる半導体装置の製造方法においては、開口部の側壁の所定の高さから層間絶縁膜の上面にかけての第１のチタン膜の上層に反応防止膜を形成した後、チタン膜とアルミニウムまたはその合金との共晶反応を起こしているので、反応するＴｉ量の制御ができ、その結果共晶反応の制御が可能になり、開口部への上部導電層の埋め込み精度が向上する。

【００３２】この発明の請求項５に係わる半導体装置の製造方法においては、反応防止膜をチタンの窒化膜、酸化膜または窒酸化膜としたので、下層のチタン膜と上層のアルミニウムまたはその合金膜との共晶反応を完全に防止できる。

【００３３】この発明の請求項６に係わる半導体装置の製造方法においては、各膜をスパッタ法で形成したので、精度よく成膜できる。

【００３４】この発明の請求項７に係わる半導体装置の製造方法においては、大気暴露することなく連続的に行うので、各膜の表面に自然酸化膜が形成されない。従って、成膜反応や共晶反応が妨害されることがない。

【図面の簡単な説明】

【図１】　この発明の実施の形態１に係わる半導体装置を説明するための断面図である。

【図２】　この発明の実施の形態１に係わる半導体装置の製造方法の一工程を説明するための断面図である。

【図３】　この発明の実施の形態１に係わる半導体装置の製造方法の一工程を説明するための断面図である。

【図４】　この発明の実施の形態１に係わる半導体装置の製造方法の一工程を説明するための断面図である。

【図５】　この発明の実施の形態１に係わる半導体装置の製造方法の一工程を説明するための断面図である。

【図６】　この発明の実施の形態１に係わる半導体装置の製造方法の一工程を説明するための断面図である。

【図７】　この発明の実施の形態１に係わる半導体装置

の製造方法の一工程を説明するための断面図である。

【図８】　この発明の実施の形態１に係わる半導体装置の製造方法の一工程を説明するための断面図である。

【図９】　従来例に係わる半導体装置を説明するための断面図である。

【図１０】　従来例に係わる半導体装置の製造方法の一工程を説明するための断面図である。

【図１１】　従来例に係わる半導体装置の製造方法の一工程を説明するための断面図である。

【図１２】　従来例に係わる半導体装置を説明するため＊の断面図である。

＊10

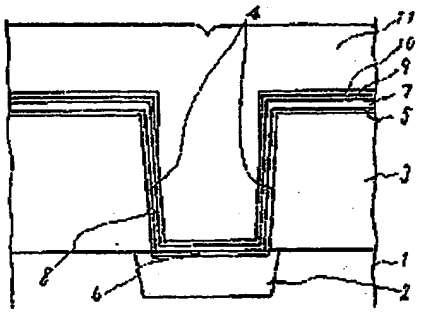
【図１３】　従来例に係わる半導体装置を説明するための断面図である。

【図１４】　従来例に係わる半導体装置を説明するための断面図である。

【符号の説明】

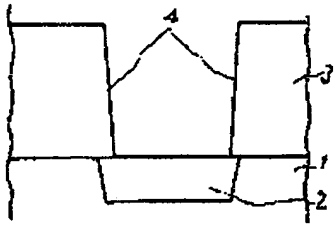
１　基板、３　層間絶縁膜、４　コンタクトホール、５　第２のＴｉ膜、６　チタンシリサイド層、７　ＴｉＮ膜、８　共晶膜、１０　ＴｉＮ膜、１１　第１のＡｌ膜、１２　第２のＡｌ膜。

【図１】

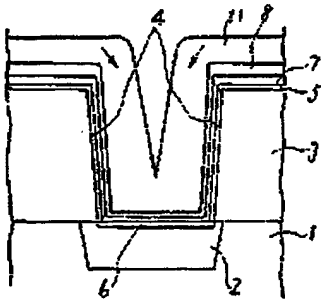


１：基板　　７：ＴｉＮ膜
３：層間絶縁膜　　８：共晶膜
４：コンタクトホール　　９：第１のＴｉ膜
５：第２のＴｉ膜　　１０：ＴｉＮ膜
６：チタンシリサイド層　　１１：第１のＡｌ膜

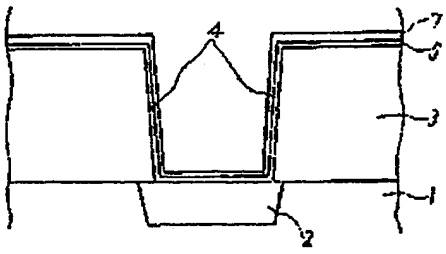
【図２】



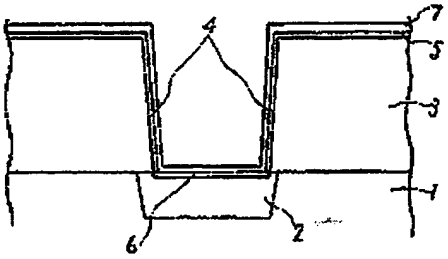
【図１１】



【図３】



【図４】



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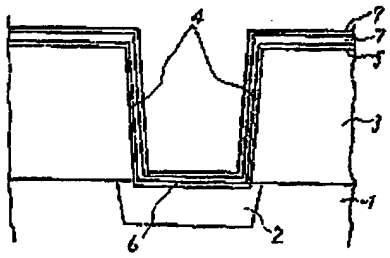
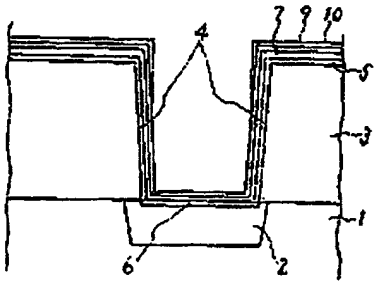


【図６】



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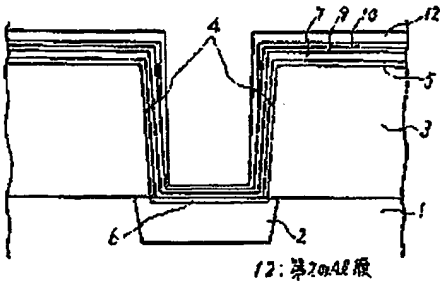
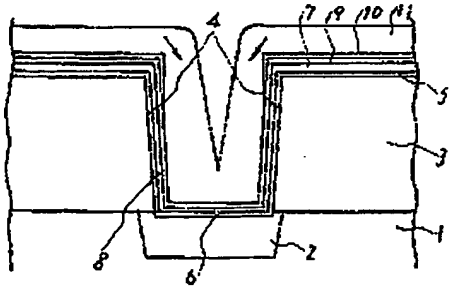


【図8】



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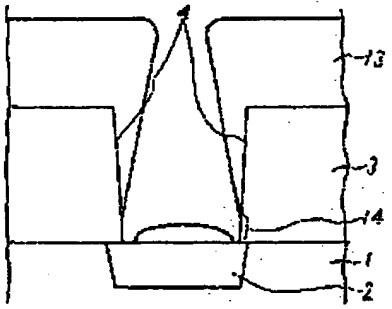
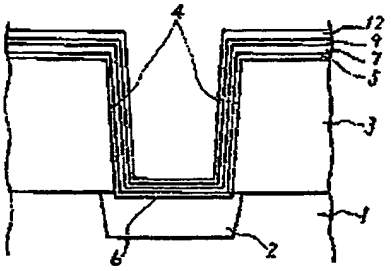


【図10】



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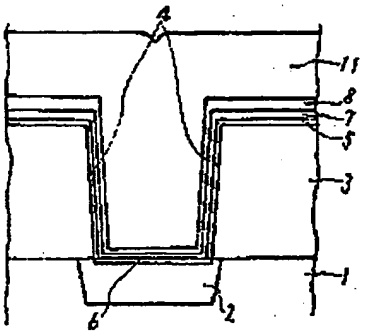
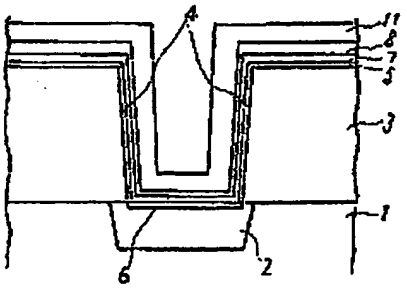


【図13】



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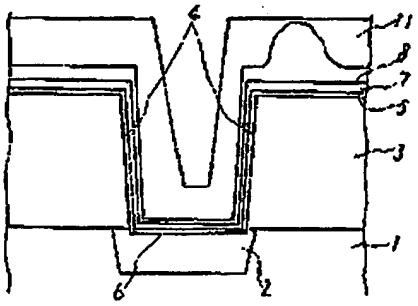

フロントページの続き

(51)Int.Cl.°	識別記号	庁内整理番号	FI	技術表示箇所
			H01L 21/90	D

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1] In the semiconductor device equipped with the up conductive layer which the interlayer insulation film was formed in the upper layer of a lower conductive layer, and opening was formed in said interlayer insulation film, embedded the conductor at said opening, and was electrically connected with said lower conductive layer The titanium with which said up conductive layer was formed even in the predetermined height of a side attachment wall from the pars basilaris ossis occipitalis of said opening, aluminum, or the eutectic film with the alloy, A cascade screen with the reaction prevention film which prevents an eutectic reaction with the 1st titanium film which was missing from the top face of said interlayer insulation film, and was formed sequentially from the lower layer from the predetermined height of the side attachment wall of said opening, said 1st titanium film, aluminum, or its alloy, The semiconductor device characterized by consisting of the 1st aluminum formed in the upper layer of said cascade screen and said eutectic film, or its alloy film.

[Claim 2] The semiconductor device according to claim 1 with which the reaction prevention film is characterized by being the nitride, the oxide film, or ******** of titanium.

[Claim 3] The semiconductor device according to claim 1 or 2 characterized by forming a titanium silicide layer in the surface section of the lower conductive layer which the 2nd titanium film has exposed to the pars basilaris ossis occipitalis of opening, respectively, forming a titanium nitride in the upper layer of said 2nd titanium film and said titanium silicide layer, and forming a cascade screen and the eutectic film in the upper layer of said titanium nitride at the upper layer of an interlayer insulation film.

[Claim 4] The process which forms an interlayer insulation film in the upper layer of a lower conductive layer, and the process which forms opening in the position of said interlayer insulation film, The process which forms the reaction prevention film in the upper layer of said 1st titanium film covered over the top face of said interlayer insulation film from the predetermined height of the process which forms the 1st titanium film all over including the interior of said opening, and the side attachment wall of said opening, The process which forms the 2nd aluminum or its alloy film in the upper layer of said 1st titanium film and said reaction prevention film, The manufacture approach of the semiconductor device which equipped even the predetermined height of a side attachment wall with the process which forms the eutectic film with titanium, aluminum, or its alloy film from the pars basilaris ossis occipitalis of said opening while forming the 1st aluminum or its alloy film in the upper layer of said 2nd aluminum or its alloy film.

[Claim 5] The manufacture approach of a semiconductor device according to claim 4 that the reaction prevention film is characterized by being the nitride, the oxide film, or ******** of titanium.

[Claim 6] The manufacture approach of a semiconductor device according to claim 4 or 5 that the formation approach of the 1st titanium film, the reaction prevention film, the 1st aluminum or its alloy film and the 2nd aluminum, or its alloy film is characterized by being a spatter.

[Claim 7] The manufacture approach of the semiconductor device according to claim 4 to 6 characterized by performing continuously all processes until it forms the 1st aluminum or its alloy film from the 1st titanium film, without carrying out atmospheric-air exposure.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the structure and its manufacture approach of the conductive layer formed in the side attachment wall of opening formed in the interlayer insulation film about a semiconductor device and its manufacture approach.
[0002]
[Description of the Prior Art] The aspect ratio of opening (for example, contact hole which is the connection hole of a semi-conductor substrate and the conductive layer formed in the upper part) by which the internal wiring makes it detailed and is used for the electric connection during each internal wiring with high integration of a semiconductor device (especially LSI) is increasing steadily.
[0003] When the aluminum which is a conductive layer, or its alloy film (it is hereafter described as aluminum film.) was formed by the conventional spatter to such high aspect ratio opening (it is hereafter described as a contact hole.), as shown in drawing 9 , the stage piece 14 arose on the aluminum film 13 inside the contact hole 4, and there was a problem that a circuit did not operate normally.
[0004] In order to solve such a problem, the elevated-temperature aluminum spatter technique was developed. Drawing 12 is the sectional view of a semiconductor device in which the aluminum film 11 was formed by the conventional elevated-temperature aluminum spatter technique. drawing -- setting -- 1 -- a semi-conductor substrate (it is hereafter described as a substrate.), and 2 -- an impurity diffused layer and 3 -- for the titanium film (it is hereafter described as Ti film.), and 6, as for the titanium nitride film (it is hereafter described as the TiN film.), and 8, a titanium silicide layer and 7 are [an interlayer insulation film and 4 / a contact hole and 5 / titanium, aluminum or the eutectic film (it is hereafter described as the eutectic film. with the alloy, and 11] aluminum film.
[0005] Moreover, the manufacture approach of the conventional semiconductor device forms the Ti film 5 and the TiN film 7 by the spatter all over including the interior of a contact hole 4, after forming an impurity diffused layer 2, an interlayer insulation film 3, and a contact hole 4 in the main front face of a substrate 1. Next, after heat-treating, making the Ti film 5 and substrate 1 which were formed in the pars basilaris ossis occipitalis of a contact hole 4 react and forming the titanium silicide layer 6, the Ti film 9 and the aluminum film 12 are formed in the upper layer of the TiN film 7 by the spatter (refer to drawing 10).
[0006] Next, the aluminum film 11 is formed in the whole surface by the spatter, heating a substrate 1 to an elevated temperature. At this time, since the aluminum film 11 and 12 is heated near the melting point, it begins to liquefy. Moreover, if the Ti film 9 and the aluminum film 12 participate in coincidence and a lifting and the aluminum film 11 begin to participate an eutectic reaction in this reaction, wettability will improve, and it will become easy to move and will go to a contact hole 4 (refer to drawing 11). And finally a contact hole 4 is embedded, flattening of the front face is carried out by the surface tension of the aluminum film 11, and it serves as a configuration shown in drawing 12 .
[0007]
[Problem(s) to be Solved by the Invention] However, with the conventional elevated-temperature aluminum spatter technique, if there are few eutectic reactions of the aluminum film 12 and the Ti film 9, by the time the aluminum film 11 goes to a contact hole 4, an eutectic reaction will stop, and as shown in drawing 13 , the embedding of a contact hole 4 will become imperfect. Moreover, the film is prevented from the aluminum film 11 which most aluminum film 11 turns into the eutectic film 8, and moves decreasing, if an eutectic reaction progresses superfluously, and this serving as a wall, if the eutectic film 8 becomes superfluous partially, and aluminum moving [11] to a contact hole 4. Therefore, as shown in drawing 14 , the embedding of a contact hole becomes imperfect. Thus, it was difficult for control of an eutectic reaction to perform embedding with a difficult and sufficient precision.
[0008] This invention was made in order to solve the above troubles, and it aims at offering the structure and its manufacture approach of the semiconductor device which can embed a conductive layer with a sufficient precision at high aspect ratio opening.
[0009]
[Means for Solving the Problem] As for the semiconductor device concerning claim 1 of this invention, an

interlayer insulation film is formed in the upper layer of a lower conductive layer. It is the semiconductor device equipped with the up conductive layer which opening was formed in said interlayer insulation film, embedded the conductor at said opening, and was electrically connected with said lower conductive layer. The titanium with which said up conductive layer was formed even in the predetermined height of a side attachment wall from the pars basilaris ossis occipitalis of said opening, aluminum, or the eutectic film with the alloy, A cascade screen with the reaction prevention film which prevents an eutectic reaction with the 1st titanium film which was missing from the top face of said interlayer insulation film, and was formed sequentially from the lower layer from the predetermined height of the side attachment wall of said opening, said 1st titanium film, aluminum, or its alloy, It consists of the 1st aluminum formed in the upper layer of said cascade screen and said eutectic film, or its alloy film.

[0010] In claim 1, the reaction prevention film of the semiconductor device concerning claim 2 of this invention is the nitride, the oxide film, or ******** of titanium.

[0011] A titanium silicide layer is formed in the surface section of a lower conductive layer by which the 2nd titanium film has exposed the semiconductor device concerning claim 3 of this invention to the pars basilaris ossis occipitalis of opening in claims 1 or 2 at the upper layer of an interlayer insulation film, respectively, a titanium nitride is formed in the upper layer of said 2nd titanium film and said titanium silicide layer, and a cascade screen and the eutectic film are formed in the upper layer of said titanium nitride.

[0012] The manufacture approach of the semiconductor device concerning claim 4 of this invention The process which forms an interlayer insulation film in the upper layer of a lower conductive layer, and the process which forms opening in the position of said interlayer insulation film, The process which forms the reaction prevention film in the upper layer of said 1st titanium film covered over the top face of said interlayer insulation film from the predetermined height of the process which forms the 1st titanium film all over including the interior of said opening, and the side attachment wall of said opening, The process which forms the 2nd aluminum or its alloy film in the upper layer of said 1st titanium film and said reaction prevention film, Even the predetermined height of a side attachment wall is equipped with the process which forms the eutectic film with titanium, aluminum, or its alloy film from the pars basilaris ossis occipitalis of said opening at the same time it forms the 1st aluminum or its alloy film in the upper layer of said 2nd aluminum or its alloy film.

[0013] In claim 4, the reaction prevention film of the manufacture approach of the semiconductor device concerning claim 5 of this invention is the nitride, the oxide film, or ******** of titanium.

[0014] In claims 4 or 5, the formation approach of the 1st titanium film, the reaction prevention film, the 1st aluminum or its alloy film and the 2nd aluminum, or its alloy film of the manufacture approach of the semiconductor device concerning claim 6 of this invention is a spatter.

[0015] The manufacture approach of the semiconductor device concerning claim 7 of this invention is continuously performed in claim 4 thru/or either of 6, without carrying out atmospheric-air exposure of all the processes until it forms the 1st aluminum or its alloy film from the 1st titanium film.

[0016]

[Embodiment of the Invention]

The gestalt 1 of operation of this invention is explained with reference to a drawing below gestalt 1. of operation. Drawing 1 is the sectional view of the semiconductor device concerning the gestalt 1 of operation. In drawing, an impurity diffused layer and 3 the substrate whose 1 is a lower conductive layer, and 2 An interlayer insulation film, 6 is the contact hole where opening of 4 was carried out to the upper interlayer insulation film 3 of an impurity diffused layer 2, Ti film whose 5 is 2nd Ti film, and Ti film (it does not illustrate.) formed in the pars basilaris ossis occipitalis of a contact hole. The titanium silicide layer which the substrate 1 reacted and was formed, Ti film the eutectic film and whose 9 7 is 1st Ti film as for the TiN film and 8, the TiN film whose 10 is the reaction prevention film, and 11 are aluminum film which is the 1st aluminum film. In addition, the titanium silicide layer 6 forms ohmic contact, and makes good contact nature of a substrate 1 and the aluminum film 11, and the TiN film 7 is a barrier layer for preventing the junction destruction by the interaction of the aluminum film 11 and a substrate 1 in the pars basilaris ossis occipitalis of a contact hole, as for the eutectic film 8, it raises the wettability of the aluminum film 11 at the time of formation, and improves embedding to a contact hole 4. Moreover, as long as the TiN film 10 is film which prevents an eutectic reaction, it may be any of the titanium oxide film or **********.

[0017] Drawing 2 -8 and drawing 1 are the sectional views of the semiconductor device in which the process was shown for the manufacture approach of the semiconductor device concerning the gestalt 1 of operation one by one later on.

[0018] As shown in drawing 2 , an interlayer insulation film 3 is formed on the main front face of the substrate 1 with which the impurity diffused layer 2 is formed, and then a contact hole 4 is formed in the upper interlayer insulation film 3 of an impurity diffused layer 2.

[0019] Next, as shown in drawing 3 , the Ti film 5 (the number of thickness 10nm) and the TiN film 7 (ten thickness - 100nm of numbers) are formed by the spatter all over including the interior of a contact hole 4.

[0020] Next, as shown in drawing 4 , heat-treat (700-800 degrees C), the Ti film 5 and substrate 1 which were formed in the pars basilaris ossis occipitalis of a contact hole 4 are made to react, and the titanium silicide layer 6 is formed.

[0021] Next, as shown in drawing 5 , the Ti film 9 (the number of thickness 10nm) is formed in the upper layer of

the TiN film 7 by the spatter.

[0022] Next, as shown in drawing 6 , the TiN film 10 is usually formed in the upper layer of the Ti film 9 by the spatter. Since step coverage nature of a spatter is usually inadequate at this time, inside a contact hole 4, membranes are formed by making thickness small (for example, 5nm or less) by only the upper part more than the predetermined height of a side attachment wall.

[0023] Next, as shown in drawing 7 , the aluminum film 12 (the number of thickness 100nm) which is the 2nd aluminum film is formed in the whole surface by the spatter. [0024] Next, the aluminum film 11 (the number of thickness 100nm) is formed in the whole surface by the spatter, heating a substrate 1 to an elevated temperature (about 500 degrees C), as shown in drawing 8 . At this time, the aluminum film 11 goes to a contact hole 4 by the wettability improvement by the eutectic reaction of the aluminum film 12 and the Ti film 9, and liquefaction by heating, finally a contact hole 4 is embedded, flattening of the front face is carried out by the surface tension of the aluminum film 11, and it serves as a configuration shown in drawing 1 . In addition, since the TiN film 10 is formed, an eutectic reaction is produced only in the part which the Ti film 9 below contact hole 4 side-attachment-wall fixed height has exposed (eutectic film 8).

[0025] The membrane formation conditions in the gestalt 1 of this operation are shown below.

Ti film formation condition DC power Several kW process gas Ar Number 10SCCM pressure Number 10-1PaTiN film formation condition DC power Several kW process gas Ar/N2 10/number 10SCCM pressure of numbers Number 10-1PaAl film formation condition DC power Several kW process gas Ar Number 10SCCM pressure Ten to 1 Pa number [0026] As mentioned above, since the TiN film 10 which is reaction prevention film was alternatively formed in the top face of an interlayer insulation film 3, and the upper part of the side attachment wall of the contact hole 4 interior, only the Ti film 9 which has exposed the contact hole 4 interior reacts with the aluminum film 12. Therefore, a superfluous eutectic reaction can be prevented. Moreover, since the Ti film's 9 which reacts existence part is limited, the amount of Ti which reacts by controlling the thickness of the Ti film 9 of the part is controllable. Therefore, control of an eutectic reaction is attained and can embed a contact hole with a sufficient precision by the aluminum film 11.

[0027] In addition, since the spatter of step coverage nature was usually inadequate in formation with the Ti film 5 and 9 and the TiN film 7, in order to improve step coverage nature, the collimation spatter method was used. Moreover, although this invention was used for the contact hole with the gestalt 1 of operation, if it is high aspect ratio opening, it can be adapted similarly about the veer hole which is a connection hole between the conductive layers of a lower layer and the upper layer.

[0028]

[Effect of the Invention] In the semiconductor device concerning claim 1 of this invention, since the reaction prevention film is formed in the upper layer of the 1st titanium film covered over the top face of an interlayer insulation film from the predetermined height of the side attachment wall of opening, control of an eutectic reaction with titanium, aluminum, or its alloy is attained, and the embedding precision of the up conductive layer to opening improves.

[0029] In the semiconductor device concerning claim 2 of this invention, since the reaction prevention film was made into the nitride, the oxide film, or ******** of titanium, an eutectic reaction can be prevented completely.

[0030] In the semiconductor device concerning claim 3 of this invention, since the nitride of titanium is formed between a lower conductive layer, titanium, aluminum, or the eutectic film with that alloy, the mutual reaction of a lower conductive layer and aluminum is controlled, and junction destruction can be prevented.

[0031] since the eutectic reaction with a titanium film , aluminum , or its alloy be cause after forming a reaction prevention film in the upper layer of the 1st titanium film cover over the top face of an interlayer insulation film from the predetermined height of the side attachment wall of opening , can perform control of the amount of Ti which react , as a result , control of an eutectic reaction be attain , and the embedding precision of the up conductive layer to opening improve in the manufacture approach of the semiconductor device concerning claim 4 of this invention .

[0032] In the manufacture approach of the semiconductor device concerning claim 5 of this invention, since the reaction prevention film was made into the nitride, the oxide film, or ******** of titanium, the lower layer titanium film, the upper aluminum, or an eutectic reaction with that alloy film can be prevented completely.

[0033] In the manufacture approach of the semiconductor device concerning claim 6 of this invention, since each film was formed by the spatter, membranes can be formed with a sufficient precision.

[0034] In the manufacture approach of the semiconductor device concerning claim 7 of this invention, since it carries out continuously, without carrying out atmospheric-air exposure, the natural oxidation film is not formed in the front face of each film. Therefore, neither a membrane formation reaction nor an eutectic reaction is blocked.

[Translation done.]

* NOTICES *

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TECHNICAL FIELD

[Field of the Invention] Especially this invention relates to the structure and its manufacture approach of the conductive layer formed in the side attachment wall of opening formed in the interlayer insulation film about a semiconductor device and its manufacture approach.

[Translation done.]

* NOTICES *

PRIOR ART

[Description of the Prior Art] The aspect ratio of opening (for example, contact hole which is the connection hole of a semi-conductor substrate and the conductive layer formed in the upper part) by which the internal wiring makes it detailed and is used for the electric connection during each internal wiring with high integration of a semiconductor device (especially LSI) is increasing steadily.

[0003] When the aluminum which is a conductive layer, or its alloy film (it is hereafter described as aluminum film.) was formed by the conventional spatter to such high aspect ratio opening (it is hereafter described as a contact hole.), as shown in drawing 9 , the stage piece 14 arose on the aluminum film 13 inside the contact hole 4, and there was a problem that a circuit did not operate normally.

[0004] In order to solve such a problem, the elevated-temperature aluminum spatter technique was developed. Drawing 12 is the sectional view of a semiconductor device in which the aluminum film 11 was formed by the conventional elevated-temperature aluminum spatter technique. drawing -- setting -- 1 -- a semi-conductor substrate (it is hereafter described as a substrate.), and 2 -- an impurity diffused layer and 3 -- for the titanium film (it is hereafter described as Ti film.), and 6, as for the titanium nitride film (it is hereafter described as the TiN film.), and 8, a titanium silicide layer and 7 are [an interlayer insulation film and 4 / a contact hole and 5 / titanium, aluminum or the eutectic film (it is hereafter described as the eutectic film. with the alloy, and 11] aluminum film.

[0005] Moreover, the manufacture approach of the conventional semiconductor device forms the Ti film 5 and the TiN film 7 by the spatter all over including the interior of a contact hole 4, after forming an impurity diffused layer 2, an interlayer insulation film 3, and a contact hole 4 in the main front face of a substrate 1. Next, after heat-treating, making the Ti film 5 and substrate 1 which were formed in the pars basilaris ossis occipitalis of a contact hole 4 react and forming the titanium silicide layer 6, the Ti film 9 and the aluminum film 12 are formed in the upper layer of the TiN film 7 by the spatter (refer to drawing 10).

[0006] Next, the aluminum film 11 is formed in the whole surface by the spatter, heating a substrate 1 to an elevated temperature. At this time, since the aluminum film 11 and 12 is heated near the melting point, it begins to liquefy. Moreover, if the Ti film 9 and the aluminum film 12 participate in coincidence and a lifting and the aluminum film 11 begin to participate an eutectic reaction in this reaction, wettability will improve, and it will become easy to move and will go to a contact hole 4 (refer to drawing 11). And finally a contact hole 4 is embedded, flattening of the front face is carried out by the surface tension of the aluminum film 11, and it serves as a configuration shown in drawing 12 .

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention] In the semiconductor device concerning claim 1 of this invention, since the reaction prevention film is formed in the upper layer of the 1st titanium film covered over the top face of an interlayer insulation film from the predetermined height of the side attachment wall of opening, control of an eutectic reaction with titanium, aluminum, or its alloy is attained, and the embedding precision of the up conductive layer to opening improves.

[0029] In the semiconductor device concerning claim 2 of this invention, since the reaction prevention film was made into the nitride, the oxide film, or ******** of titanium, an eutectic reaction can be prevented completely.

[0030] In the semiconductor device concerning claim 3 of this invention, since the nitride of titanium is formed between a lower conductive layer, titanium, aluminum, or the eutectic film with that alloy, the mutual reaction of a lower conductive layer and aluminum is controlled, and junction destruction can be prevented.

[0031] since the eutectic reaction with a titanium film , aluminum , or its alloy be cause after forming a reaction prevention film in the upper layer of the 1st titanium film cover over the top face of an interlayer insulation film from the predetermined height of the side attachment wall of opening , can perform control of the amount of Ti which react , as a result , control of an eutectic reaction be attain , and the embedding precision of the up conductive layer to opening improve in the manufacture approach of the semiconductor device concerning claim 4 of this invention .

[0032] In the manufacture approach of the semiconductor device concerning claim 5 of this invention, since the reaction prevention film was made into the nitride, the oxide film, or ******** of titanium, the lower layer titanium film, the upper aluminum, or an eutectic reaction with that alloy film can be prevented completely.

[0033] In the manufacture approach of the semiconductor device concerning claim 6 of this invention, since each film was formed by the spatter, membranes can be formed with a sufficient precision.

[0034] In the manufacture approach of the semiconductor device concerning claim 7 of this invention, since it carries out continuously, without carrying out atmospheric-air exposure, the natural oxidation film is not formed in the front face of each film. Therefore, neither a membrane formation reaction nor an eutectic reaction is blocked.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, with the conventional elevated-temperature aluminum spatter technique, if there are few eutectic reactions of the aluminum film 12 and the Ti film 9, by the time the aluminum film 11 goes to a contact hole 4, an eutectic reaction will stop, and as shown in drawing 13 , the embedding of a contact hole 4 will become imperfect. Moreover, the film is prevented from the aluminum film 11 which most aluminum film 11 turns into the eutectic film 8, and moves decreasing, if an eutectic reaction progresses superfluously, and this serving as a wall, if the eutectic film 8 becomes superfluous partially, and aluminum moving [11] to a contact hole 4. Therefore, as shown in drawing 14 , the embedding of a contact hole becomes imperfect. Thus, it was difficult for control of an eutectic reaction to perform embedding with a difficult and sufficient precision.

[0008] This invention was made in order to solve the above troubles, and it aims at offering the structure and its manufacture approach of the semiconductor device which can embed a conductive layer with a sufficient precision at high aspect ratio opening.

[Translation done.]

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MEANS

[Means for Solving the Problem] As for the semiconductor device concerning claim 1 of this invention, an interlayer insulation film is formed in the upper layer of a lower conductive layer. It is the semiconductor device equipped with the up conductive layer which opening was formed in said interlayer insulation film, embedded the conductor at said opening, and was electrically connected with said lower conductive layer. The titanium with which said up conductive layer was formed even in the predetermined height of a side attachment wall from the pars basilaris ossis occipitalis of said opening, aluminum, or the eutectic film with the alloy, A cascade screen with the reaction prevention film which prevents an eutectic reaction with the 1st titanium film which was missing from the top face of said interlayer insulation film, and was formed sequentially from the lower layer from the predetermined height of the side attachment wall of said opening, said 1st titanium film, aluminum, or its alloy, It consists of the 1st aluminum formed in the upper layer of said cascade screen and said eutectic film, or its alloy film.

[0010] In claim 1, the reaction prevention film of the semiconductor device concerning claim 2 of this invention is the nitride, the oxide film, or ******** of titanium.

[0011] A titanium silicide layer is formed in the surface section of a lower conductive layer by which the 2nd titanium film has exposed the semiconductor device concerning claim 3 of this invention to the pars basilaris ossis occipitalis of opening in claims 1 or 2 at the upper layer of an interlayer insulation film, respectively, a titanium nitride is formed in the upper layer of said 2nd titanium film and said titanium silicide layer, and a cascade screen and the eutectic film are formed in the upper layer of said titanium nitride.

[0012] The manufacture approach of the semiconductor device concerning claim 4 of this invention The process which forms an interlayer insulation film in the upper layer of a lower conductive layer, and the process which forms opening in the position of said interlayer insulation film, The process which forms the reaction prevention film in the upper layer of said 1st titanium film covered over the top face of said interlayer insulation film from the predetermined height of the process which forms the 1st titanium film all over including the interior of said opening, and the side attachment wall of said opening, The process which forms the 2nd aluminum or its alloy film in the upper layer of said 1st titanium film and said reaction prevention film, Even the predetermined height of a side attachment wall is equipped with the process which forms the eutectic film with titanium, aluminum, or its alloy film from the pars basilaris ossis occipitalis of said opening at the same time it forms the 1st aluminum or its alloy film in the upper layer of said 2nd aluminum or its alloy film.

[0013] In claim 4, the reaction prevention film of the manufacture approach of the semiconductor device concerning claim 5 of this invention is the nitride, the oxide film, or ******** of titanium.

[0014] In claims 4 or 5, the formation approach of the 1st titanium film, the reaction prevention film, the 1st aluminum or its alloy film and the 2nd aluminum, or its alloy film of the manufacture approach of the semiconductor device concerning claim 6 of this invention is a spatter.

[0015] The manufacture approach of the semiconductor device concerning claim 7 of this invention is continuously performed in claim 4 thru/or either of 6, without carrying out atmospheric-air exposure of all the processes until it forms the 1st aluminum or its alloy film from the 1st titanium film.

[0016]

[Embodiment of the Invention]

The gestalt 1 of operation of this invention is explained with reference to a drawing below gestalt 1. of operation. Drawing 1 is the sectional view of the semiconductor device concerning the gestalt 1 of operation. In drawing, an impurity diffused layer and 3 the substrate whose 1 is a lower conductive layer, and 2 An interlayer insulation film, 6 is the contact hole where opening of 4 was carried out to the upper interlayer insulation film 3 of an impurity diffused layer 2, Ti film whose 5 is 2nd Ti film, and Ti film (it does not illustrate.) formed in the pars basilaris ossis occipitalis of a contact hole. The titanium silicide layer which the substrate 1 reacted and was formed, Ti film the eutectic film and whose 9 7 is 1st Ti film as for the TiN film and 8, the TiN film whose 10 is the reaction prevention film, and 11 are aluminum film which is the 1st aluminum film. In addition, the titanium silicide layer 6 forms ohmic contact, and makes good contact nature of a substrate 1 and the aluminum film 11, and the TiN film 7 is a barrier layer for preventing the junction destruction by the interaction of the aluminum film 11 and a substrate 1 in the pars basilaris ossis occipitalis of a contact hole, as for the eutectic film 8, it raises the wettability of the aluminum film 11 at the time of formation, and improves embedding to a contact hole 4. Moreover, as long as the TiN film 10

is film which prevents an eutectic reaction, it may be any of the titanium oxide film or **********.

[0017] Drawing 2 -8 and drawing 1 are the sectional views of the semiconductor device in which the process was shown for the manufacture approach of the semiconductor device concerning the gestalt 1 of operation one by one later on.

[0018] As shown in drawing 2 , an interlayer insulation film 3 is formed on the main front face of the substrate 1 with which the impurity diffused layer 2 is formed, and then a contact hole 4 is formed in the upper interlayer insulation film 3 of an impurity diffused layer 2.

[0019] Next, as shown in drawing 3 , the Ti film 5 (the number of thickness 10nm) and the TiN film 7 (ten thickness - 100nm of numbers) are formed by the spatter all over including the interior of a contact hole 4.

[0020] Next, as shown in drawing 4 , heat-treat (700-800 degrees C), the Ti film 5 and substrate 1 which were formed in the pars basilaris ossis occipitalis of a contact hole 4 are made to react, and the titanium silicide layer 6 is formed.

[0021] Next, as shown in drawing 5 , the Ti film 9 (the number of thickness 10nm) is formed in the upper layer of the TiN film 7 by the spatter.

[0022] Next, as shown in drawing 6 , the TiN film 10 is usually formed in the upper layer of the Ti film 9 by the spatter. Since step coverage nature of a spatter is usually inadequate at this time, inside a contact hole 4, membranes are formed by making thickness small (for example, 5nm or less) by only the upper part more than the predetermined height of a side attachment wall.

[0023] Next, as shown in drawing 7 , the aluminum film 12 (the number of thickness 100nm) which is the 2nd aluminum film is formed in the whole surface by the spatter.

[0024] Next, the aluminum film 11 (the number of thickness 100nm) is formed in the whole surface by the spatter, heating a substrate 1 to an elevated temperature (about 500 degrees C), as shown in drawing 8 . At this time, the aluminum film 11 goes to a contact hole 4 by the wettability improvement by the eutectic reaction of the aluminum film 12 and the Ti film 9, and liquefaction by heating, finally a contact hole 4 is embedded, flattening of the front face is carried out by the surface tension of the aluminum film 11, and it serves as a configuration shown in drawing 1 . In addition, since the TiN film 10 is formed, an eutectic reaction is produced only in the part which the Ti film 9 below contact hole 4 side-attachment-wall fixed height has exposed (eutectic film 8).

[0025] The membrane formation conditions in the gestalt 1 of this operation are shown below.

Ti film formation condition DC power Several kW process gas Ar Number 10SCCM pressure Number 10-1PaTiN film formation condition DC power Several kW process gas Ar/N2 10/number 10SCCM pressure of numbers Number 10-1PaAl film formation condition DC power Several kW process gas Ar Number 10SCCM pressure Ten to 1 Pa number [0026] As mentioned above, since the TiN film 10 which is reaction prevention film was alternatively formed in the top face of an interlayer insulation film 3, and the upper part of the side attachment wall of the contact hole 4 interior, only the Ti film 9 which has exposed the contact hole 4 interior reacts with the aluminum film 12. Therefore, a superfluous eutectic reaction can be prevented. Moreover, since the Ti film's 9 which reacts existence part is limited, the amount of Ti which reacts by controlling the thickness of the Ti film 9 of the part is controllable. Therefore, control of an eutectic reaction is attained and can embed a contact hole with a sufficient precision by the aluminum film 11.

[0027] In addition, since the spatter of step coverage nature was usually inadequate in formation with the Ti film 5 and 9 and the TiN film 7, in order to improve step coverage nature, the collimation spatter method was used. Moreover, although this invention was used for the contact hole with the gestalt 1 of operation, if it is high aspect ratio opening, it can be adapted similarly about the veer hole which is a connection hole between the conductive layers of a lower layer and the upper layer.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is a sectional view for explaining the semiconductor device concerning the gestalt 1 of implementation of this invention.
[Drawing 2] It is a sectional view for explaining one process of the manufacture approach of the semiconductor device concerning the gestalt 1 of implementation of this invention.
[Drawing 3] It is a sectional view for explaining one process of the manufacture approach of the semiconductor device concerning the gestalt 1 of implementation of this invention.
[Drawing 4] It is a sectional view for explaining one process of the manufacture approach of the semiconductor device concerning the gestalt 1 of implementation of this invention.
[Drawing 5] It is a sectional view for explaining one process of the manufacture approach of the semiconductor device concerning the gestalt 1 of implementation of this invention.
[Drawing 6] It is a sectional view for explaining one process of the manufacture approach of the semiconductor device concerning the gestalt 1 of implementation of this invention.
[Drawing 7] It is a sectional view for explaining one process of the manufacture approach of the semiconductor device concerning the gestalt 1 of implementation of this invention.
[Drawing 8] It is a sectional view for explaining one process of the manufacture approach of the semiconductor device concerning the gestalt 1 of implementation of this invention.
[Drawing 9] It is a sectional view for explaining the semiconductor device concerning the conventional example.
[Drawing 10] It is a sectional view for explaining one process of the manufacture approach of the semiconductor device concerning the conventional example.
[Drawing 11] It is a sectional view for explaining one process of the manufacture approach of the semiconductor device concerning the conventional example.
[Drawing 12] It is a sectional view for explaining the semiconductor device concerning the conventional example.
[Drawing 13] It is a sectional view for explaining the semiconductor device concerning the conventional example.
[Drawing 14] It is a sectional view for explaining the semiconductor device concerning the conventional example.
[Description of Notations]
1 A substrate, 3 An interlayer insulation film, 4 A contact hole, 5 2nd Ti film, 6 A titanium silicide layer, 7 The TiN film, 8 The eutectic film, 10 The TiN film, 11 1st aluminum film, 12 2nd aluminum film.

[Translation done.]

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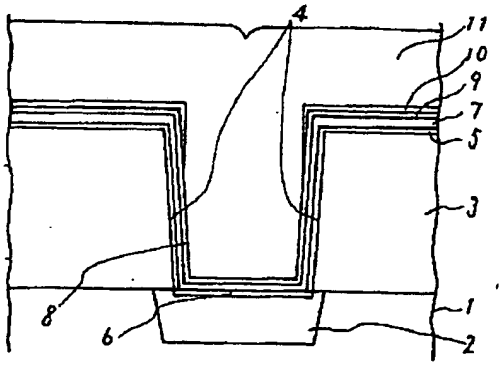
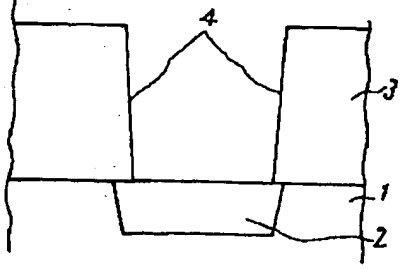
DRAWINGS

[Drawing 1]

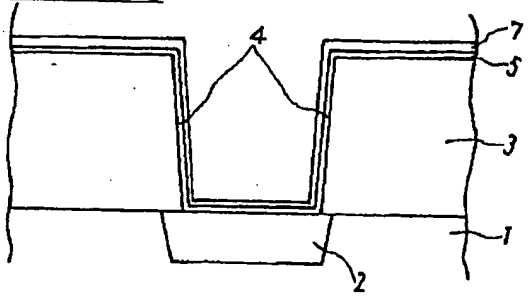


1：基板　7：TiN膜
3：層間絶縁膜　8：共晶膜
4：コンタクトホール　9：第1のTi膜
5：第2のTi膜　10：TiN膜
6：チタンシリサイド層　11：第1のAl膜

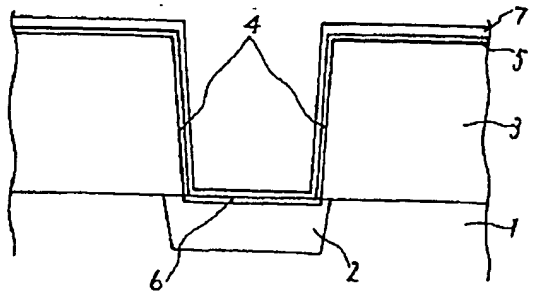
[Drawing 2]



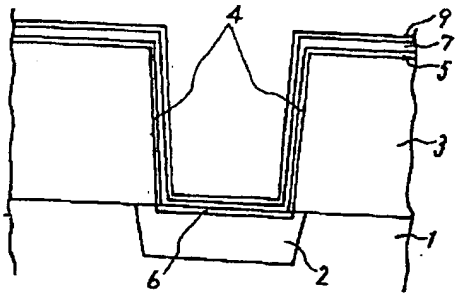
[Drawing 3]



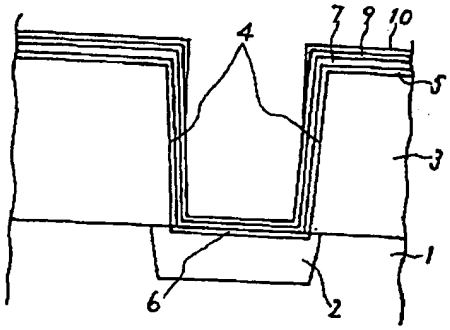
[Drawing 4]



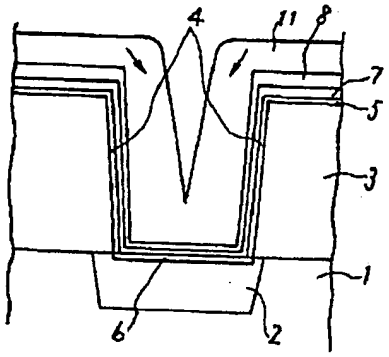
[Drawing 5]



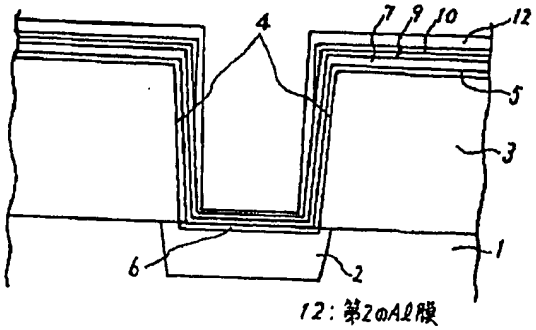
[Drawing 6]



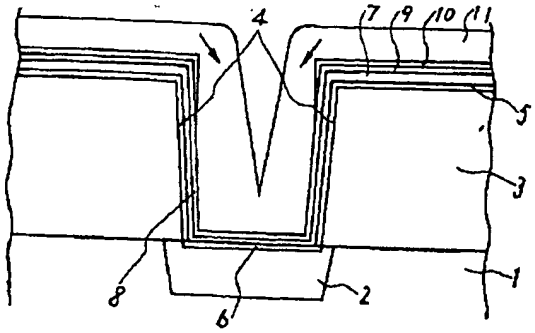
[Drawing 11]



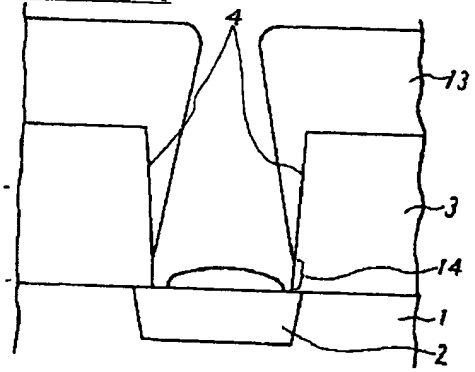
[Drawing 7]



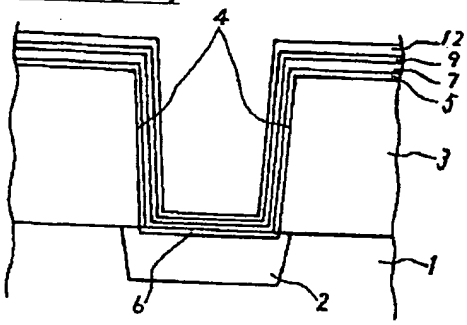
[Drawing 8]



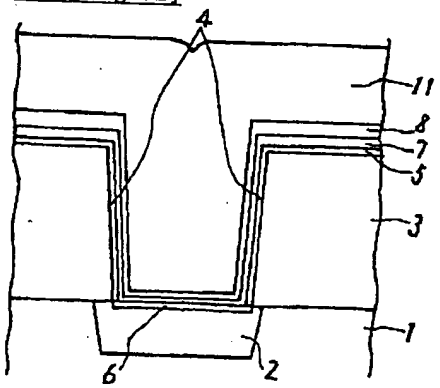
[Drawing 9]



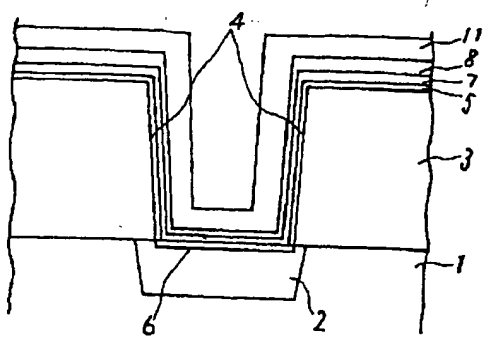
[Drawing 10]



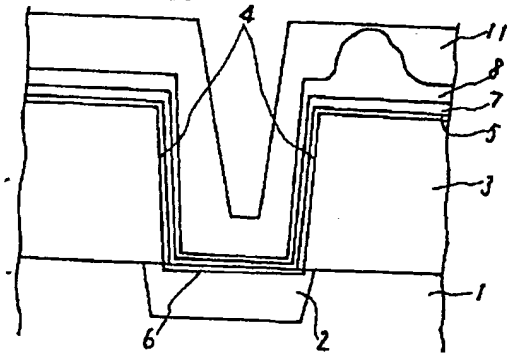
[Drawing 12]



[Drawing 13]



[Drawing 14]



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